

Concurrency theory

Exercise sheet 10

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Out: January 24

Due: January 30

Submit your solutions until Wednesday, January 30, 12:00am.

Exercise 1

Consider two traces $\tau = \alpha.a.b.\gamma$ and $\tau' = \alpha'.a.\beta.b.\gamma'$ where $\text{thread}(c) \neq \text{thread}(a)$ and $\text{thread}(c) \neq \text{thread}(b)$ for all c in β . Prove the following:

If $a \rightarrow_{\text{hb}} b$ in $\text{Tr}_{\text{TSO}}(\tau)$ then $a \rightarrow_{\text{hb}}^+ b$ in $\text{Tr}_{\text{TSO}}(\tau')$

Exercise 2

Consider the following program implementing an instance of the **non-blocking write** protocol by H. Kopetz and J. Reisinger:

$\ell_1 : h \leftarrow \text{mem}[g]; \text{ goto } \ell_2$	$\ell_9 : h \leftarrow \text{mem}[g]; \text{ goto } \ell_{10}$
$\ell_2 : \text{mem}[g] \leftarrow h + 1; \text{ goto } \ell_3$	$\ell_{10} : \text{mem}[g] \leftarrow h + 1; \text{ goto } \ell_{11}$
$\ell_3 : \text{mem}[x] \leftarrow 42; \text{ goto } \ell_4$	$\ell_{11} : \text{mem}[x] \leftarrow 43; \text{ goto } \ell_{12}$
$\ell_4 : \text{mem}[g] \leftarrow h + 2; \text{ goto } \ell_5$	$\ell_{12} : \text{mem}[g] \leftarrow h + 2;$
$\ell_5 : r \leftarrow \text{mem}[g]; \text{ goto } \ell_6$	
$\ell_6 : v \leftarrow \text{mem}[x]; \text{ goto } \ell_7$	
$\ell_7 : s \leftarrow \text{mem}[g]; \text{ goto } \ell_8$	
$\ell_8 : \text{assert } r \neq s \vee r \text{ is odd}; \text{ goto } \ell_5$	
$\ell_8 : \text{assert } r = s \wedge r \text{ is even};$	

Note that there are two instructions labeled by ℓ_8 . Assume that when executing $\text{goto } \ell_8$, the execution non-deterministically jumps to any of them.

Prove that the program is not robust under TSO. Initially assume $\text{mem}[g] = 0$ and $g \neq x$.

Exercise 3

Consider a computation $\tau = \tau_1.act_1.\tau_2 \in \text{C}_{\text{SC}}(P)$ where for all act_2 in τ_2 we have $act_1 \rightarrow_{\text{hb}}^* act_2$. Show that the computation $\tau.act$ satisfies $act_1 \rightarrow_{\text{hb}}^* act$ if and only if

1. there is an action act_2 in $act_1.\tau_2$ with $\text{thread}(act_2) = \text{thread}(act)$, or
2. act is a load whose address is stored in $act_1.\tau_2$, or
3. act is a store (with issue) whose address is loaded or stored in $act_1.\tau_2$.